SiFive Freedom U500 Platform

Introduction

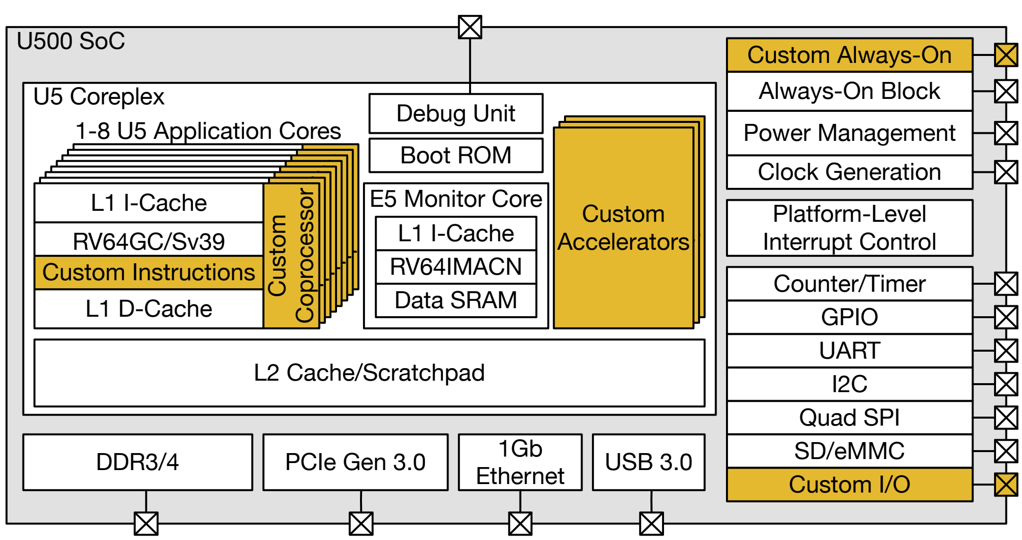
The U500 platform is the first member of SiFive's Freedom Unleashed family of customizable RISC-V SoCs. Combining a configurable high-performance Unix-capable cache-coherent 64-bit multiprocessor with application-specific custom hardware, the Freedom Unleashed family reduces NRE and time-to-market for customized SoCs in diverse markets such as machine learning, storage and networking.

Each U500 SoC can include a SiFive U5 Coreplex with 1–8 64-bit RISC-V cores with private caches and a shared L2 cache, DDR3/DDR4 DRAM channels, Dual Mode PCIe Gen 3.0, 1Gb Ethernet, USB 3.0, a platform-level interrupt controller, an on-chip debug unit, as well as an extensive selection of other peripheral devices. All aspects of the base U500 platform can be flexibly configured. In addition, the platform can be readily extended with custom instruction-set extensions, custom coprocessors, custom accelerators, custom I/O, and custom always-on blocks. The resulting customized U500 SoC is optimized for manufacture in a TSMC 28nm metal-gate process, and delivered as packaged tested parts by SiFive.

Configurable 64-bit RISC-V U5 Coreplex

The U5 RISC-V Coreplex can be configured with up to eight 64-bit cache-coherent U5 application cores. Each U5 core has a high-performance single-issue in-order 64-bit execution pipeline, with a peak sustained execution rate of one instruction per clock cycle. U5 cores include a comprehensive dynamic branch prediction scheme, including BTBs, BHTs, and return-address stacks to improve performance. The cores support the standard RV64IMAFD ISA, including full hardware support for single and double-precision IEEE 754-2008 floating-point with fully pipelined fused multiply-adders, a hardware divide and square-root unit, and full hardware support for subnormal numbers. A hardware integer multiplier and divider is also provided. The U5 core optionally supports the standard C compressed extension for reduced code size.

Each core's private L1 instruction and data caches can be configured with various sizes and associativities. The shared L2 cache can also be configured for size and associativity, and divided into interleaved banks to improve performance. The L2 also supports runtime reconfiguration between cache and scratchpad RAM uses. The L2 cache acts as the system coherence hub, with an inclusive directory-based coherence scheme to avoid



wasting bandwidth on snoops. All cache structures are protected with parity and/or ECC.

The cores implement a 512 GiB virtual address space using the Sv39 virtual address translation scheme with a hardware page-table walker to accelerate TLB refills.

U5 Coreplexes optionally include an E5-series RV64IMACN monitor core to securely boot the system and service background tasks without disturbing the larger cores. The monitor core has fully coherent access to the shared memory system and all peripherals.

The U5 Coreplex can be extended with new custom instructions that operate on the existing user registers, or with custom coprocessors implementing new instructions that operate on additional architectural state.

All SiFive U5 Coreplexes are guaranteed to be compatible with all applicable RISC-V standards.

Custom Accelerators

Custom autonomous accelerators can be added to provide application-specific processing. Custom accelerators have full coherent access to the L2 cache and DRAM subsystem, with control over cache-allocation policies for memory-resident streams. Accelerators can also generate and receive interrupts from the platform-level interrupt controller.

DRAM Subsystem

U500 SoCs can be configured with up to four 72-bit DDR3/4 DRAM channels, with full ECC support, providing up to 68 GB/s of memory bandwidth.

High-Speed I/O

U500 SoCs can be configured with a range of high-speed I/O devices, including Dual Mode PCIe Gen 3.0 with a configurable number of lanes and controllers, USB 3.0 including OTG, and Gigabit Ethernet interfaces. High-speed I/Os can master directly into the cache-coherent memory system, and can optionally allocate data directly into the shared L2 cache.

Peripheral Devices

A wide variety of peripheral devices can be chosen from a large catalog of standard components, including counter/timers, watchdogs, PWM, GPIO, UART, I2C, SPI, ADC, DAC, and SD/eMMC. Third-party peripheral IP can be attached via industry-standard SoC buses or TileLink.

Interrupt Controller

The configurable platform-level interrupt controller supports a large number of inputs and programmable priority levels, and also supports nested interrupt handling for faster interrupt response.

Always-On Block and Power Management

U500 SoCs can be configured with active power management to reduce leakage current in sleep mode. The Always-On Block (AON) supports low-power sleep with wakeup from an internal real-time clock interrupt, external I/O stimulus, or custom always-on circuitry.

Debug Support

Each U500 system includes extensive platform-level debug facilities including hardware breakpoints, watchpoints, and single-step execution accessed via an industry-standard JTAG interface and supported by a full set of open-source debug tools. All components in the system, including processors, accelerators, memories, peripheral devices, and the interrupt controller, can be controlled and monitored over the debug port.

Software Tools

SiFive provides a full open-source RISC-V software development toolchain for U500 SoCs, including a full Linux port with device drivers for the supported devices, modern C and C++ compilers, standard libraries, assemblers, linkers, together with debug tools to drive the on-chip debug hardware.

U500 FPGA Development Board

U500 FPGA boards with preconfigured designs are available to support development of software and hardware for the U500 platform. Developers can register at `dev.sifive.com`.

Further Information

On request, SiFive can provide additional information on further customization options including compute accelerators and available packaging technologies.

Proprietary Notice

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